## REMARKS

The publication number of an application referenced by serial number in the original application specification is being inserted by this Amendment in two locations.

Examined claims 10, 11 and 14-16 remain pending, the independent claims 10 and 14 being amended.

### *Claim Rejections Under 35 U.S.C. §103*

Claims 10 and 11

Independent claim 10 and its dependent claim 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over previously cited U.S. publication no. 2003/0028704 A1 to Mukaida et al. (hereinafter "Mukaida") in view of newly cited U.S. patent no. 6,721,843 B1 to Estakhri (hereinafter "Estakhri"). Claim 10 is being amended to more specifically define the invention being claimed.

The Mikaida reference has been extensively discussed in responses filed on or about March 23, 2007, October 29, 2007 and February 26, 2008, to prior office actions. In order to avoid a repetition of those rather extensive discussions, which are incorporated herein, these remarks are directed to the question of whether, given the limitation of claims 10 and 11 identified in the Office Action (sentence bridging pages 3 and 4) to be missing from Mikaida, it would have been obvious in light of newly cited Estakhri to modify Mikaida to supply that missing limitation. It is respectfully submitted that Estakhri does not describe or suggest the limitation of the claims not disclosed by Mikaida, and, for that reason, the obviousness rejection is not well taken.

The Office Action (sentence bridging pages 3 and 4) correctly points out that Mikaida does not teach a memory system that writes (1) a given one or more units of data having consecutive logical addresses sequentially into pages within individual blocks, and (2) more than said given number of units of data having consecutive logical addresses in parallel into pages within two or more blocks of one of the metablocks in two or more planes. Estakhri is then alleged in the Office Action (page 4, lines 2-11) to describe writing a given one or more units of data into pages of individual blocks and writing more than the given number of units of data in

parallel into pages of two or more blocks of a metablock. Estakhri does describe, as revealed by the portions cited in the Office Action, a memory system operating in two modes but the operating mode is selected in response to the nature of the host with which the memory system is connected, rather than by the amount of data received with a write command. No suggestion can be found in Estakhri of storing incoming data in one of two ways that depends on the number of units of data having consecutive logical addresses that are received with write commands, to which claims 10 and 11 are directed.

Estakhri describes three scenarios for operating a memory system with a host (see Estakhri, col. 17, ln. 48 – col. 18, ln. 47). The first (Estakhri, col. 17, ln. 65 – col. 18, ln. 8) is applicable to a traditional memory card, where the host defaults to the traditional configuration. In the second and third scenarios (Estakhri, col. 18, lns. 9-37), a high performance memory card sends the host a vendor unique value in order to determine the capabilities of the host. If the host does not respond by identifying itself as a high performance host, the memory card operates in a standard default mode without simultaneous programming in separate memory banks. But if the host does respond to indicate it is a high performance host, then the memory system operates in a high performance mode to store incoming data in successive memory banks.

What is missing from Estakhri is any suggestion of the memory system operating differently depending on the number of units of data having consecutive logical addresses that are received by the memory system with write commands. In Estakhri's first scenario, the memory card operates in only one way, and in the second and third scenarios, all data, no matter how much, are stored in the memory card operating in a mode that depends upon the nature of the host. None of Estakhri's three scenarios cause data to be written either in a single plane or in two or more planes, depending on the number of units of data that are received. To emphasize this difference of claims 10 and 11 over Estakhri, a step is being added by this Amendment of determining the number of units of data having consecutive logical addresses that are being received with write commands. This is described, for example, in paragraph 0041 of the present application. Such a step is certainly not part of Estakhri's memory system operation.

It is therefore respectfully submitted that Estakhri does not suggest the limitation of claims 10 and 11 that the Office Action correctly acknowledges to be missing from Mukaida.

The claims cannot therefore be held to have been obvious over Mukaida and Estakhri. The memory systems of Mikaida and Estakhri are much different from each other in ways relevant to the operation recited in claims 10 and 11.

Claims 14-16

Claims 14-16 have rejected under 35 U.S.C. § 103(a) as being unpatentable over Mukaida in view of U.S. publication no. 2004/0030825 A1 to Otake et al. (hereinafter "Otake"). The basis for the rejection appears to be the same as expressed in the previous Office Action, with the addition of a "Response to Arguments" section (Office Action, pages 7 and 8), which is appreciated.

In the responsive Amendment filed February 26, 2008 (page 6, last paragraph), the following argument was made:

> "Even if the disclosures of Mukaida or [and] Otake are fit together in some manner, such a combination would not include the option of writing *all* the received data into pages of blocks of *only one* of the sub-arrays when there is a small amount of data being written." (Emphasis in the original.)

In response to this argument, the current Office Action states that this feature is not recited in claim 14. However, attention is directed to the following limitation of claim 14:

> "in response to receiving the write commands with a number of one or more sectors of data for only a single page of data, writing all the received data in parallel into individual pages of individual blocks of only one of the sub-arrays,"

It is therefore respectfully submitted that the argued limitation is part of claim 14, and that this distinguishes any combination of Mikaida and Otake that may reasonably be argued. In Otake, data are written in parallel into two or more blocks, not into blocks of only one of multiple sub-arrays. Otake does not, therefore, disclose the above-quoted limitation of claim 14, contrary to the reason that Otake was relied upon in the Office Action.

The Office Action (page 8, lines 1-8) then argues that Mukaida describes "writing all the data received in parallel into individual pages of individual blocks of only one of the sub-arrays," referencing Mukaida's Figure 22 and paragraphs 0289-0297. However, the timing diagram of Figure 22 shows quite the opposite. The data being received are stored in four banks ##0-3 of memory cells. The data are not described to be stored in a single one of the banks but rather in

all of four of them. Mukaida does not, it is respectfully submitted, contain the disclosure relied upon to reject claim 14.

It is further alleged in the Office Action (page 8, last paragraph) that claim 14 defines a memory operation that meets either of the first **or** second conditions. This position is respectfully traversed. Claim 14 clearly recites the operation of a memory system according to either of two specific techniques, depending upon the amount of sectors of data that are received with a write command. The claimed operation is able to implement a selected one of the recited two writing techniques. One or the other is selected on the basis of the amount of data received with a write command. Claim 14 is directed to a memory system that operates according to either one of two techniques, both of which are available in the system for use.

The Office Action (page 8, lines 12-13) summarizes the way that obviousness is being determined, as follows: "Thus, one skill [skilled] in the art would recognize the combination of Mukaida and Otake teaches the claimed limitations as recited in claim 14." However, this is respectfully submitted to apply an incorrect test of obviousness under 35 U.S.C. § 103(a). The test applied in the Office Action appears to be whether one skilled in the art would now be able to find the claimed invention somewhere in the two cited references. But the correct test is whether one ordinarily skilled in the art would have found the invention to be obvious at the time the present invention was made (at least as early as the December 30, 2003 filing date of the present application), without first having knowledge of the present application or invention.

For the foregoing reasons, it is respectfully submitted that claims 14-16 are patentable.

***Information Disclosure Statements***

The Office Action (page 2) acknowledges that the Supplemental Information Disclosure Statement filed February 26, 2008 has been considered by the Examiner, which is appreciated. However, the form 1449 returned with the current Office Action is from another Supplemental Information Disclosure Statement that was filed December 12, 2007. Since the form 1449 of the February 26, 2008 Statement has three additional U.S. patents listed that are not present on the form 1449 returned with the Office Action, consideration of these additional three references and the return of the February 26th form 1449 initialed by the Examiner are respectfully requested.

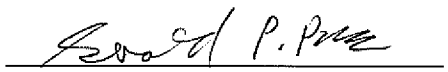
Additionally, a further Supplemental Information Disclosure Statement is being filed herewith.

***Conclusion***

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-276-6534 would be appreciated.

**FILED VIA EFS**

Respectfully submitted,



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